

ABSTRACT OF THE DISCLOSURE

The present invention provides a semiconductor integrated circuit device capable of reading memory information from an on-chipped nonvolatile memory cell transistor at high speed. The memory cell transistor includes, in a first well region, a pair of memory electrodes of which one serves as a source electrode and the other serves as a drain electrode, and a channel region interposed between the pair of memory electrodes, and includes, on a channel region, a first gate electrode disposed near its corresponding memory electrode with an insulating film interposed therebetween, and a second gate electrode disposed through insulating films and a charge storage region and electrically isolated from the first gate electrode. A first negative voltage is applied to the first well region to form a state of a reverse bias greater than or equal to a junction withstand voltage between the second gate electrode and the memory electrode near the second gate electrode, thereby enabling injection of hot electrons into the charge storage region and injection of electrons from the well region to the charge storage region.